ARM Cordio-B50 stack

Overview

The ARM® Cordio® stack is designed specifically for Bluetooth® low energy single-mode products catering to the power sensitive Internet of Things (IoT) market. With its small code size, easy-to-use APIs, and portable architecture, the Cordio stack is a superior solution for companies looking to develop Bluetooth low energy semiconductors while reducing time-to-market.

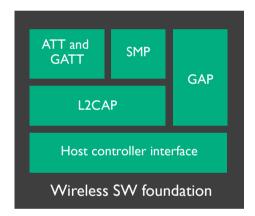
The stack will be qualification tested and for compliance with the latest version of the Bluetooth 5 core specification.

Cordio stack consists of:

- Generic Attribute Protocol (GATT) and Attribute Protocol (ATT): efficient data transactions
- Generic Access Profile (GAP): Connection and device management
- Security Manager Protocol (SMP): Pairing and authentication
- L2CAP: Streamlined data transport
- HCI: "Thin" HCl or full transport-based HCl
- Wireless Software Foundation (WSF): Portable OS services and wrappers.

Key features:

- Ease of use: APIs designed with applications in mind – optimized for battery powered resource constrained devices
- Efficient memory usage: Designed for minimum RAM and code size (as small as 10KB)
- Full featured: Supports master and slave operation (central and peripheral), client and server, multiple simultaneous connections
- Modular: Include or exclude features as needed
- Bluetooth qualified subsystem
- Portable: Unique Wireless Software
 Foundation (WSF) layer enables easy
 porting to any microcontroller or
 operating system. Proven on embedded
 processors like the ARM Cortex®-M
 processor series.

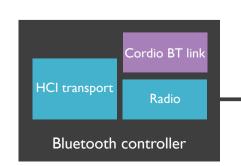


Single chip solution

Single and dual-chip solutions:

"Thin" software HCl layer for single-chip. Standard transport-based HCl for dual-chip.

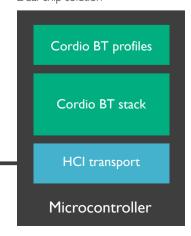
In a single-chip system the Cordio stack runs on the processor inside the SoC. A "thin" HCl layer simply adapts to the software interface of the target's LE link layer. In a dual-chip system the Cordio stack runs on a microcontroller and communicates with a Bluetooth low





energy controller chip over a wired interface such as UART or SPI. A standard transport-based HCI layer manages the communication between the two devices.

Dual-chip solution





Radio core IP

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